PATENT ABSTRACTS OF JAPAN

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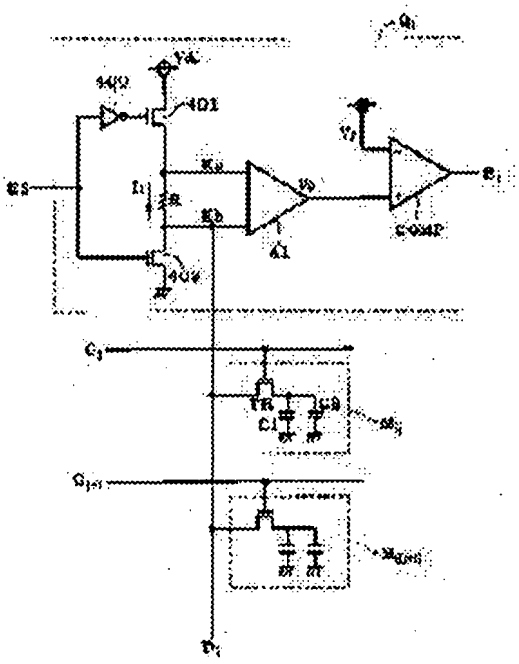
(54) PRESSURE DETECTING DIGITIZER

(57)Abstract:

PROBLEM TO BE SOLVED: To provide a technique for realizing a function as a tablet by detecting the pressure applied to a liquid crystal display element.

SOLUTION: A detecting pulse generating circuit is activated by line- sequentially applying pulses to gate lines G1-GL. While the gate line Gj is activated, a transistor 402 is turned on by the positive pulse of a reset signal RS and a capacitor C1 and a liquid crystal C2 of a liquid crystal display cell Mij are discharged through a brain line Di. When the reset signal RS is turned into 'L', transistors 401 and 402 are respectively turned on and off and the capacitor C1 and liquid crystal C2 are charged by a power source Vdd. When the liquid crystal display cell Mij of j-th line is pressed, since the capacitance of the liquid crystal C2 is increased, it is charged with a charge amount more than the other liquid crystal display cell. Therefore, an output Vo based on a charging current Ir is increased as well and by appropriately setting a reference potential Vr, a discriminate signal Ei can be activated.



* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] Especially this invention relates to the technique which detects the local pressure to a liquid crystal display panel about a pressure detection digitizer.
[0002]
[Description of the Prior Art] The pen input panel called a tablet is proposed from the former with diversification of information machines and equipment in recent years and an advance of a handwriting recognition technique. The type with which the panel which has especially a display function is used also [panel / this / pen input] is developed.
[0003] And about this type, the so-called "hybrid system" which only piled up the tablet of various methods and the display panel from the former is adopted.
[0004]
[Problem(s) to be Solved by the Invention] However, in the hybrid system, the digitizing sheet needed to be stuck, for example on the liquid crystal display panel, and the rise of cost was caused.
[0005] Then, this invention offers the technique of realizing the function as a tablet, by detecting the pressure to a liquid crystal display component.
[0006]
[Means for Solving the Problem] Two or more gate lines by which what starts claim 1 among this invention was arranged in the 1st direction, The liquid crystal display cel which has two or more drain wires arranged in the 2nd direction, and the liquid crystal which said gate line is activated and is connected to said drain wire, and is prepared in each of the intersection of said gate line and said drain wire, It is the pressure detection digitizer equipped with the detection pulse generating circuit which it connects [pulse generating circuit] with said gate line and makes line sequential activate said gate line, and the judgment circuit which is connected to said drain wire and detects change of the electrostatic capacity of said liquid crystal for said every drain wire.
[0007] It is the pressure detection digitizer according to claim 1 which starts claim 2 among this invention, and said judgment circuit has a charge means to make said liquid crystal charge through said drain wire, and a current detection means to detect the current with which charge of said liquid crystal is presented.
[0008] It is the pressure detection digitizer according to claim 2 which starts claim 3 among this invention, and the period which said gate line activates is classified into the 2nd period following the 1st period and said 1st period, respectively, said judgment circuit is further equipped with a discharge means to make said liquid crystal discharge in said 1st period through said drain wire, and charge of said liquid crystal is performed in said 2nd period.
[0009] It is the pressure detection digitizer according to claim 3 which starts claim 4 among this invention, and said judgment circuit is further equipped with a current potential conversion means to transform into an electrical potential difference the current with which said charge is presented, the peak hold circuit which undergoes the output of said current potential conversion means, and the high-pass

filter which undergoes the output of said peak hold circuit.
[0010] It is the pressure detection digitizer according to claim 2 which starts claim 5 among this invention, and once said detection pulse generating circuits activate said all gate lines all at once in a predetermined period, they make line sequential activate said gate line.
[0011] It is the pressure detection digitizer according to claim 1 which starts claim 6 among this invention. Said judgment circuit A reference capacitor, It connects with a charge means to charge said reference capacitor while the switch which connects said reference capacitor to said drain wire, and said switch turn off, and said drain wire. It has a discharge means to discharge said liquid crystal while said switch turns off, and a detection means to detect the potential of the node of said switch and said reference capacitor.
[0012] It is the pressure detection digitizer according to claim 1 which starts claim 7 among this invention, and said judgment circuit is set at a reference capacitor and the 1st and 2nd periods. The switch which connects said reference capacitor to said drain wire, and a charge means to charge said reference capacitor while said switch turns off, It has a discharge means to discharge said liquid crystal at said 1st period, and a detection means to detect the potential of the node of said switch and said reference capacitor at said 2nd period.
[0013] It is the pressure detection digitizer according to claim 6 or 7 which starts claim 8 among this invention, and said judgment circuit is further equipped with the peak hold circuit which receives the potential of said node, and the high-pass filter which undergoes the output of said peak hold circuit.
[0014] It is claim 1 4 and 6 thru/or the pressure detection digitizer of any one publication of eight that starts claim 9 among this invention, and said detection pulse generating circuit makes line sequential activate said gate line in the blanking period about said liquid crystal display cel.
[0015]
[Embodiment of the Invention] Principle . drawing 1 of this invention is the conceptual diagram showing the configuration of the pressure detection digitizer concerning this invention. In a panel 201, drain wires D1 and D2, --, Di, --, Dn and the gate lines G1 and G2, --, Gj, --, GL cross in the shape of a matrix. For example, the liquid crystal display cel Mij is formed near the intersection of a drain wire Di and the gate line Gj, and this is equipped with Transistor TR, liquid crystal C2, and a capacitor C1. A drain is common in a drain wire Di, the source is common in a capacitor C1 and liquid crystal C2, and the gate electrode of Transistor TR is connected to the gate line Gj, respectively. The capacitor C1 is formed in order to accumulate the status signal which makes it display on liquid crystal C2. The same is said of other intersections.
[0016] A pulse is given to the gate lines G1-GL from a scanning circuit 202 line sequential, and a status signal is given to drain wires D1-Dn from a hold circuit 203.
[0017] The panel 201 constituted as mentioned above, the scanning circuit 202, and the hold circuit 203 are the same as that of the structure which it has in the usual liquid crystal display panel from the former. However, in this invention, it has further the pressure detecting circuit 205 connected to drain wires D1-Dn, and the detection pulse generating circuit 204 connected to the gate lines G1-GL.
[0018] A pulse is given to the gate lines G1-GL like [the detection pulse generating circuit 204] a scanning circuit 202 line sequential. Moreover, the detection pulse generating circuit 204 detects change of the current in drain wires D1-Dn, and an electrical potential difference, and outputs the judgment signals E1-En. The detection pulse generating circuit 204 is equipped with the judgment circuits Q1-Qn connected to drain wires D1-Dn, respectively, and the judgment signals E1-En are acquired from the judgment circuits Q1-Qn, respectively.
[0019] Drawing 2 is the cross section showing the principle of this invention. This drawing (a) shows the case where the pressure is not applied, and shows the case where this drawing (b) has required the pressure. The liquid crystal object 100 is inserted and enclosed with the up substrate 101 and the lower substrate 102, and when the pressure is not applied, it is maintained by thickness d. However, if the up substrate 101 is pressed with the pen 300 for an input and this is dented, directly under the, the liquid crystal objects 100 will decrease in number to thickness d*, and the electrostatic capacity will d/d* double. In this invention, the charge and discharge current to the liquid crystal C2 and the capacitor C1

which are invited by change of this electrostatic capacity, and change of an electrical potential difference are detected.

[0020] In addition, on these specifications, liquid crystal C2 is also grounded, and the case where it connects with a capacitor C1 and juxtaposition is taken and explained to an example. However, other fixed potentials may be given to liquid crystal C2. Moreover, in the usual liquid crystal display panel, a capacitor C1 is not indispensable in this invention like not being indispensable as for a capacitor C1.

[0021] Gestalt 1. drawing 3 of operation is the circuit diagram showing an example of the judgment circuit Qi concerning the gestalt 1 of operation of this invention. Reset-signal RS is inputted, it connects with a drain wire Di, and the judgment circuit Qi outputs the judgment signal Ei.

[0022] The judgment circuit Qi is equipped with the inverter 400 which gives logic reversal of reset-signal RS, the NMOS transistor 401 to which the output of an inverter 400 is given, the NMOS transistor 402 to which reset-signal RS is given, Resistance R and an integrator A1, and Comparator COMP. A transistor 401, Resistance R, and a transistor 402 are connected to touch-down from the power source Vdd at the serial at this order, one input edge Ka of an integrator A1 is connected with a transistor 401 at a node with Resistance R, and the input edge Kb of another side of an integrator A1 is connected with the transistor 402 at the node with Resistance R, respectively.

[0023] The input edge Kb of an integrator A1 is connected to the drain wire Di, and the outgoing end of an integrator A1 has given the output Vo to the plus input edge of Comparator COMP. The reference potential Vr is given to the negative input edge of Comparator COMP, and the judgment signal Ei is acquired from the outgoing end of Comparator COMP.

[0024] Drawing 4 is a timing chart which shows actuation of the judgment circuit Qi shown in drawing 3 . A period T2 is a period when a liquid crystal panel functions as a digitizer, and it is separately established with a display period so that it may mention later in the gestalt 7 of operation.

[0025] The detection pulse generating circuit 204 gives a pulse to the gate lines G1-GL like a scanning circuit 202 line sequential (the expression of "activating a gate line" is also used together below). And in the first stage within this pulse, reset-signal RS gives a forward pulse. The detection pulse generating circuit 204 can be made to generate this reset-signal RS.

[0026] In the period which the gate line Gj is activating, a transistor 402 is turned on by the forward pulse of reset-signal RS, and the capacitor C1 and liquid crystal C2 of the liquid crystal display cel Mij discharge through a drain wire Di. Since the transistor 401 is turned off at this time, a charge is not supplied to a capacitor C1 and liquid crystal C2 from a power source Vdd. Moreover, the input edge Kb of an integrator A1 is grounded.

[0027] If reset-signal RS is set to "L", a transistor 401,402 will turn on and turn off, respectively and a capacitor C1 and liquid crystal C2 will shift to the charge condition by the power source Vdd from a discharge condition. Since Resistance R intervenes between a transistor 401 and a drain wire Di, the charging current Ir produces a voltage drop in this resistance R, and an output Vo is obtained when an integrator integrates with this electrical potential difference.

[0028] Since considering the case where liquid crystal display cel M<SUB>ij of the j-th line is pressed now the capacity of liquid crystal C2 increases rather than the liquid crystal C2 of other liquid crystal display cels, it charges in many amount of charges rather than other liquid crystal display cels. Although the input edge Kb of an integrator A1 produces a potential rise periodically according to a gate line being activated to line sequential as shown in drawing 4 since it connects also with the liquid crystal display cel of other lines, it becomes more remarkable than the period which other gate lines are activating in the period which the gate line Gj is activating. Therefore, an output Vo can also become large and the judgment signal Ei can be activated by setting up the reference potential Vr suitably.

[0029] It can recognize which line the location of a press part is by being able to recognize which train the location of a press part is by any of the judgment signals E1-En were activated as mentioned above, and contrasting the time of day which the judgment signal activated, and the time of day which the gate line activated. And since a liquid crystal display cel is adopted as a component of pressure detection, it is not necessary to stick a digitizing sheet on a liquid crystal display panel, and the rise of cost can be controlled. Furthermore, the abbreviation of wiring is possible if the line which receives the line and

signal which give a pulse for pressure detection like the gestalt of this operation is made to serve a double purpose with the gate lines G1-GL and drain wires D1-Dn for a display. Of course, the line which receives the line and signal which give a pulse for pressure detection may be separately formed with the gate lines G1-GL for a display, and drain wires D1-Dn.

[0030] Gestalt 2. drawing 5 of operation is the circuit diagram showing a part of judgment circuit Qi concerning the gestalt 2 of operation of this invention. The circuit for processing the output Vo obtained by the configuration shown in drawing 3 , and acquiring the judgment signal Ei is illustrated, and it permutes by the comparator COMP in drawing 3 .

[0031] When the pressure from the outside to a liquid crystal panel is weak, change of the electrostatic capacity of liquid crystal C2 becomes small, and by the judgment by the reference potential Vr, also when cannot detect press or incorrect-detecting it, it thinks.

[0032] With the gestalt of this operation, after having given the output Vo to the peak hold circuit 301, obtaining the output V1, giving this further to the high-pass filter 302 and obtaining an output V2, a buffer 303 is given and it operates orthopedically, and the judgment signal Ei is acquired.

[0033] Drawing 6 is a timing chart which shows actuation of the gestalt of this operation. Even if change of an output Vo is minute, it is detected by the peak hold circuit 301 that the peak value changed, and an output V1 starts. The standup of this output V1 is made steep with a high-pass filter 302, and an output V2 is obtained.

[0034] With the gestalt of this operation, signal level can be enlarged [in / as mentioned above / the gestalt 1 of operation] to a noise etc., and incorrect detection can be avoided.

[0035] Gestalt 3. drawing 7 of operation. Reset-signal RS is inputted, it connects with a drain wire Di, and the judgment circuit Qi outputs the judgment signal Ei.

[0036] As compared with the configuration shown in drawing 3 in the gestalt 1 of operation, the inverter 400 for reversing a transistor 401,402 and reset-signal RS is deleted, and it has the composition of having added instead the transistor 403 controlled by reset-signal RS between the plus input edge of Comparator COMP, and touch-down.

[0037] Drawing 8 is a timing chart which shows actuation of the gestalt of this operation. With the gestalt of this operation, the beginning of the period T2 when a liquid crystal panel functions as a digitizer is made to once activate the gate lines G1-GL all at once altogether, and all the capacitors C1 and liquid crystal C2 of the liquid crystal display cels Mi1-MiL in i train are charged according to the power source Vdd through Resistance R. Since it is dependent on the magnitude of the status signal given by then to each liquid crystal display cels Mi1-MiL, in what kind of curve the potential of the input edge Kb of an integrator A1 reaches potential Vdd at this time covers with the slash by a diagram.

[0038] Once activating the gate lines G1-GL all at once altogether, it makes line sequential activate the gate lines G1-GL like the gestalt 1 of operation. Since the amount of charges accumulated in the capacitor C1 and liquid crystal C2 which it has will increase if the liquid crystal display cel Mij of j lines of the capacitor C1 of the liquid crystal display cels Mi1-MiL and the liquid crystal C2 is pressed once potential Vdd charges, when the gate line Gj is activated, the charging current Ir flows Resistance R again from a power source Vdd. Since the liquid crystal display cel Mij which is not pressed is already charged on the electrical potential difference Vdd even if a corresponding gate line is activated, the charging current does not flow anew.

[0039] Since the charging current Ir for the second time reduces the potential of the input edge Kb of an integrator A1 for the voltage drop in Resistance R, only when the gate line Gj corresponding to the pressed liquid crystal display cel Mij is activated, the reference potential Vr can be set up so that an output Vo may exceed the reference potential Vr.

[0040] However, reset-signal RS generates a forward pulse immediately after activating the gate lines G1-GL to line sequential, a transistor 403 turns on, and the plus input edge of Comparator COMP is grounded whenever the gate lines G1-GL are activated to line sequential. Therefore, when the following gate line was activated, potential became zero compulsorily, and the output Vo of the integrator A1 corresponding to the pressed liquid crystal display cel Mij has prevented incorrect detection.

[0041] The pressed part can be recognized [in / as mentioned above / the gestalt of this operation] like

the gestalt 1 of operation. Of course, an output Vo may be processed as it is shown in the gestalt 2 of operation.

[0042] Gestalt 4. drawing 9 of operation is the circuit diagram showing an example of the judgment circuit Qi concerning the gestalt 4 of operation of this invention. Reset-signal RS is inputted, it connects with a drain wire Di, and the judgment circuit Qi outputs the judgment signal Ei.

[0043] The judgment circuit Qi is equipped with the inverter 407 which gives logic reversal of reset-signal RS, the NMOS transistor 406 to which the output of an inverter 407 is given, the NMOS transistor 404,405 to which reset-signal RS is given, the reference capacitor 501, and Comparator COMP.

[0044] The drain of a transistor 404,406 is connected to a drain wire Di in common, and the source of a transistor 404 is grounded. A power source Vdd is connected to the drain of a transistor 405, and the reference capacitor 501 is connected to the transistor 405 at juxtaposition. The source of a transistor 405,406 is connected to the negative input edge of Comparator COMP in common, the reference potential Vr is given to the plus input edge of Comparator COMP, and the judgment signal Ei is acquired from an outgoing end.

[0045] Drawing 10 is a timing chart which shows actuation of the gestalt of this operation. After the gate lines G1-GL are activated to line sequential in a period T2 and each gate line is activated like the gestalt 1 of operation, reset-signal RS presents a forward pulse.

[0046] By the forward pulse of reset-signal RS, a transistor 404,405 turns on and the capacitor C1 of the liquid crystal display cel Mij, discharge of liquid crystal C2, and discharge of the reference capacitor 501 are performed, respectively. Under the present circumstances, since the transistor 406 is turned off, the drain wire Di and the negative input edge of Comparator COMP are insulated, and the potential Vc of the negative input edge of Comparator COMP turns into the power-source potential Vdd.

[0047] Then, reset-signal RS is set to "L", a transistor 406 turns on, the negative input edge of Comparator COMP is connected to a drain wire Di, and the reference capacitor 501 is connected to a serial to the parallel connection object of the capacitor C1 and liquid crystal C2 in the liquid crystal display cel Mij.

[0048] Therefore, after potential Vc rises rapidly to the power-source potential Vdd when a transistor 405 short-circuits while reset-signal RS presents a forward pulse, it is fallen and attached to the partial pressure determined as the reference capacitor 501 by the capacity factor with the above-mentioned parallel connection object.

[0049] However, in the period which the gate line Gj activates, since the capacity of the above-mentioned parallel connection object in the pressed liquid crystal display cel Mij is increasing as compared with other liquid crystal display cels, potential Vc falls greatly rather than it can set at the period which activates other gate lines. Therefore, the judgment signal Ei can be acquired by comparing potential Vc with the reference potential Vr with Comparator COMP.

[0050] Gestalt 5. drawing 11 of operation is the circuit diagram showing a part of judgment circuit Qi concerning the gestalt 5 of operation of this invention. The circuit for processing the output Vc obtained by the configuration shown in drawing 9 , and acquiring the judgment signal Ei is illustrated, and it permutes by the comparator COMP in drawing 9 .

[0051] The ballet hold circuit 304 which is a hold circuit to the peak of a negative side inputs potential Vc, holds the minimum value, and obtains an output V3. Furthermore, this is given to a high-pass filter 305, an output V4 is obtained, and an output V4 inputs into the clock edge (falling detection) of D flip-flop 306. The power source Vdd which supplies the potential equivalent to logic"H", for example, a power source, is connected to D input edge of D flip-flop 306. The output V5 obtained from Q outgoing end of D flip-flop 306 is inputted into other input edges of the AND gate 307 which has the input edge to which the gate lines G1-GL were connected, and acquires the judgment signal Ei from the AND gate 307.

[0052] Drawing 12 is a timing chart which shows actuation of the gestalt of this operation. Even if reduction of potential Vc is minute, it is detected by the ballet hold circuit 304 that the minimum value (ballet value) changed, and an output V3 falls. Falling of this output V3 is made steep with a high-pass

filter 305, and an output V4 is obtained. D flip-flop 306 makes an output V5 "H" in falling of an output V4, and the AND gate 307 is opened. Thereby, the potential of the activated gate line Gj appears in the judgment signal Ei as a pulse.

[0053] With the gestalt of this operation, signal level can be enlarged to a noise etc. and incorrect detection can be avoided [in / as mentioned above / the gestalt 4 of operation].

[0054] Gestalt 6. drawing 13 of operation is the circuit diagram showing an example of the judgment circuit Qi concerning the gestalt 6 of operation of this invention. Reset-signal RS and gate signals Za, Zb, and Zc are inputted, it connects with a drain wire Di, and the judgment circuit Qi outputs the judgment signal Ei.

[0055] The judgment circuit Qi is equipped with the NMOS transistor 405,408,409,410, the reference capacitor 501, and Comparator COMP. Reset-signal RS is given to the gate of a transistor 405, the source is grounded with the end of the reference capacitor 501, and the drain is connected to the other end of the reference capacitor 501. And a transistor 408 is connected between a drain wire Di and the other end of the reference capacitor 501, and a gate signal Zb is given. A transistor 409 is connected between a power source Vdd and the other end of the reference capacitor 501, and a gate signal Za is given. A transistor 410 is connected between the negative input edge of Comparator COMP, and the other end of the reference capacitor 501, and a gate signal Zc is given. The reference potential Vr is given to the plus input edge of Comparator COMP, and the judgment signal Ei is acquired from an outgoing end.

[0056] Drawing 14 is a timing chart which shows actuation of the gestalt of this operation. After the gate lines G1-GL are activated to line sequential in a period T2 and each gate line is activated like the gestalt 1 of operation, reset-signal RS presents a forward pulse. Potential of the other end of the reference capacitor 501 is set to Vc, and the potential of the negative input edge of Comparator COMP is expressed as Va.

[0057] Gate signals Za, Zb, and Zc are exclusively activated within limits which each gate line activates. A gate signal Za carries out fixed period activation, after reset-signal RS presents a forward pulse. A gate signal Zb is activated in the part which it is in the first half of the 1st period when reset-signal RS presents a forward pulse, and the 2nd period which is a fixed period after a gate signal Za suspends activation. The 2nd gate signal Zc is activated to a part of second half of the 2nd period.

[0058] While a certain gate line is being activated, in the 1st period, corresponding liquid crystal C1 and a corresponding capacitor C2 discharge with a transistor 405,408, the reference capacitor 501 discharges and potential Vc falls even to touch-down potential. Since gate signals Zb and Zc are not being activated while a gate signal Za presents a forward pulse and is being activated after that, the transistor 405,408,410 is turned off altogether and the transistor 409 turns it on. Thereby, the reference capacitor 501 is charged according to a power source Vdd through a transistor 409, and potential Vc rises to a power source Vdd.

[0059] Then, if a gate signal Zb is activated, since gate signals Za and Zc will not be activated, a transistor 405,409,410 is turned off altogether and a transistor 408 turns it on. Thereby, the charge which the reference capacitor 501 was accumulating moves to a capacitor C1 and a parallel connection object with liquid crystal C2 through a drain wire.

[0060] Although migration of this charge brings about the fall of potential Vc, as explained in the gestalt 4 of operation, it is fallen and attached to the partial pressure determined as the reference capacitor 501 by the capacity factor with the above-mentioned parallel connection object.

[0061] However, in the period which the gate line Gj activates, since the capacity of the above-mentioned parallel connection object in the pressed liquid crystal display cel.Mij is increasing as compared with other liquid crystal display cels, potential Vc falls greatly rather than it can set at the period which activates other gate lines.

[0062] Then, when a gate signal Zc is activated, only a transistor 410 turns on, potential Vc turns into potential Va, it is transmitted to Comparator COMP, and the judgment signal Ei can be acquired by comparing with the reference potential Vr. By the timing chart shown in drawing 14 , in order to charge the parasitic capacitance of the negative input edge of Comparator COMP because a transistor 410 turns

on, it is shown that potential Vc decreases slightly. Moreover, for charge of this parasitic capacitance, in case a transistor 410 begins to turn on potential Va (namely, when a gate signal Zc starts), it rises partly, and signs that parasitic capacitance discharges and potential Va decreases with time amount progress are also shown. However, it is possible to set up the reference potential Vr suitably and to make the existence or nonexistence of press reflect in the judgment signal Ei according to increase of the capacity in the pressed liquid crystal display cel Mij, since potential Va decreases further.

[0063] Moreover, if the parasitic capacitance of the negative input edge of Comparator COMP can be disregarded, a transistor 410 may be omitted and a gate signal Za may be activated on a gate signal Zb and an exclusion target also not using a gate signal Zc. In this case, the 1st period and 2nd period will continue.

[0064] Of course, in the gestalt of this operation, processing shown with the gestalt 5 of operation may be performed to potential Va instead of Comparator COMP.

[0065] Although not restricted in the gestalt 7. above of operation especially about the period T2 when a liquid crystal panel functions as a digitizer, except the mode shown in the gestalt 3 of operation, a period T2 can be established by turns [the period T1 and by turns] as which a liquid crystal panel displays.

[0066] Drawing 15 is a timing chart which shows actuation of the gestalt of this operation. A period T2 can use the blanking period established between [of the display period T1 of a liquid crystal panel] plurality. Also in the display period T1, a pulse is given to the gate lines G1-GL line sequential also in the period T2 which functions as a digitizer using a blanking period. However, in each of periods T1 and T2, a scanning circuit 202 and the detection pulse generating circuit 204 take charge of activation of such a line sequential gate line.

[0067] Thus, if pressure detection is performed using a blanking period, the display will not be barred even if it adopts liquid crystal as a pressure detector element.

[0068] In addition, in the mode shown in the gestalt 3 of operation, it is desirable to establish completely separately [the display period T1] the period T2 when a liquid crystal panel functions as a digitizer. It is because it is necessary to once charge all at once to all liquid crystal display cels so that it may be explained in the gestalt 3 of operation, and if a liquid crystal display cel is made to demonstrate a display function after that, it is because the effectiveness made to charge all at once is checked.

[0069]

[Effect of the Invention] Since change of the electrostatic capacity of the liquid crystal prepared in the shape of a matrix for the display is detected according to the pressure detection digitizer applied to claim 1 among this invention, the location of the liquid crystal with which it was pressed and electrostatic capacity increased is detected, with it functions also as a tablet. Therefore, it is not necessary to prepare a digitizing sheet separately with a liquid crystal display panel, and the rise of cost can be controlled.

[0070] Since the current charged by the liquid crystal with which it was pressed and electrostatic capacity increased detects a large thing as compared with the current charged by the liquid crystal which is not pressed according to the pressure detection digitizer applied to claim 2 and claim 3 among this invention, the location of the pressed liquid crystal is detectable.

[0071] When fluctuation arises at the peak of the charging current produced in case it charges one by one and the liquid crystal display cel of the 1st direction goes corresponding to the gate line activated to line sequential according to the pressure detection digitizer applied to claim 4 among this invention, according to this changed peak, a high-pass filter generates a pulse. Therefore, the judgment of the existence or nonexistence of press is strong in a noise, and stops being able to malfunction easily.

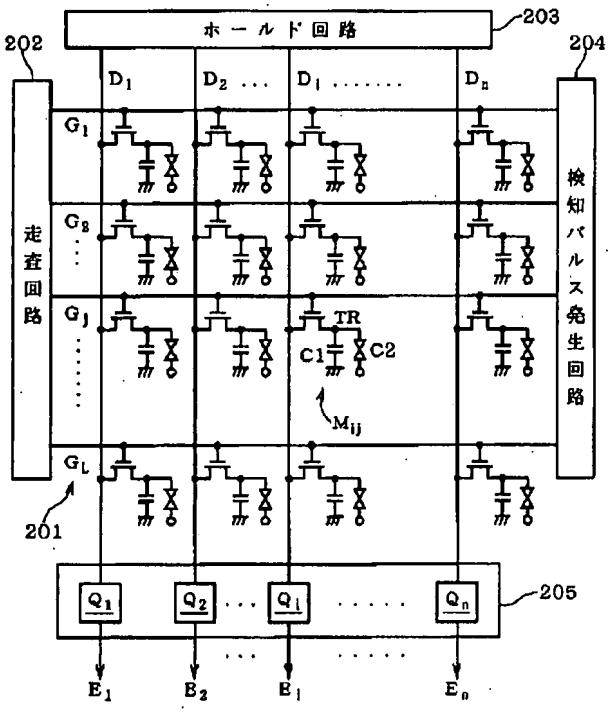
[0072] According to the pressure detection digitizer applied to claim 5 among this invention, since all liquid crystal is once charged, the charging current for the second time over the liquid crystal which it was pressed after that and electrostatic capacity increased is detectable.

[0073] According to the pressure detection digitizer applied to claim 6 and claim 7 among this invention, a reference capacitor is once charged with a charge means, liquid crystal is discharged, and it switches on after that, and is made to flow through between both. Since the potential of a node is determined with the electrostatic capacity of a reference capacitor and liquid crystal, change of the electrostatic capacity of liquid crystal is detectable by detecting this potential.

[0074] When fluctuation arises at the peak of the potential of a node produced in case it charges one by one and the liquid crystal display cel of the 1st direction goes corresponding to the gate line activated to line sequential according to the pressure detection digitizer applied to claim 8 among this invention, according to this changed peak, a high-pass filter generates a pulse. Therefore, the judgment of the existence or nonexistence of press is strong in a noise, and stops being able to malfunction easily.
[0075] According to the pressure detection digitizer applied to claim 9 among this invention, since pressure detection is performed using a blanking period, that display is not barred even if it adopts liquid crystal as a pressure detector element.

[Translation done.]

Drawing selection drawing 1

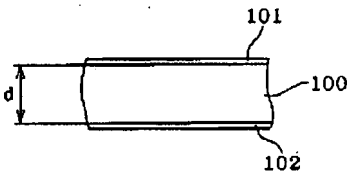


$G_1 \sim G_L$：ゲート線　　C2：液　晶
$D_1 \sim D_n$：ドレイン線　　M_{ij}：液晶表示セル
$Q_1 \sim Q_n$：出力判定回路　　205：圧力検知回路

[Translation done.]

Drawing selection drawing 2

(a)



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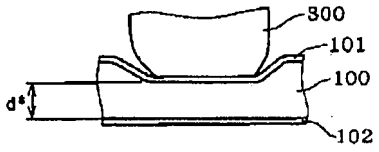
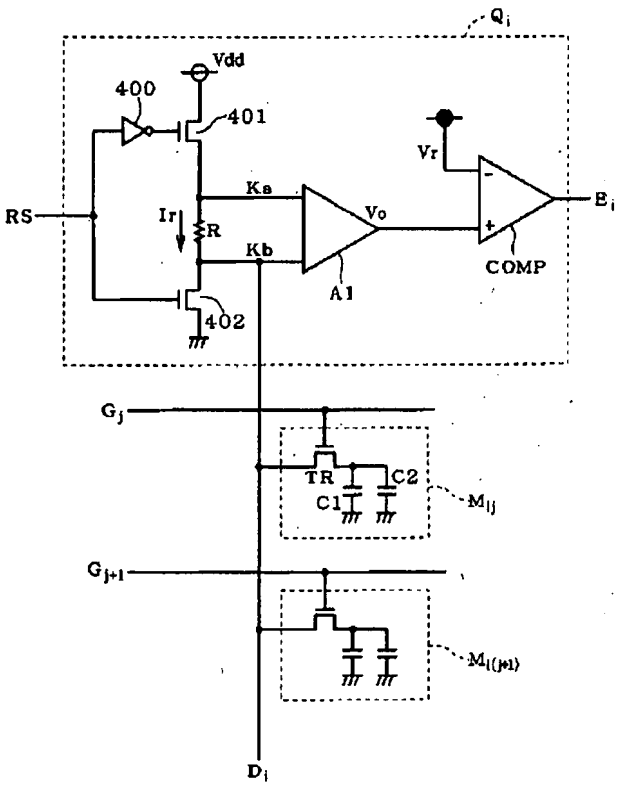


[Translation done.]

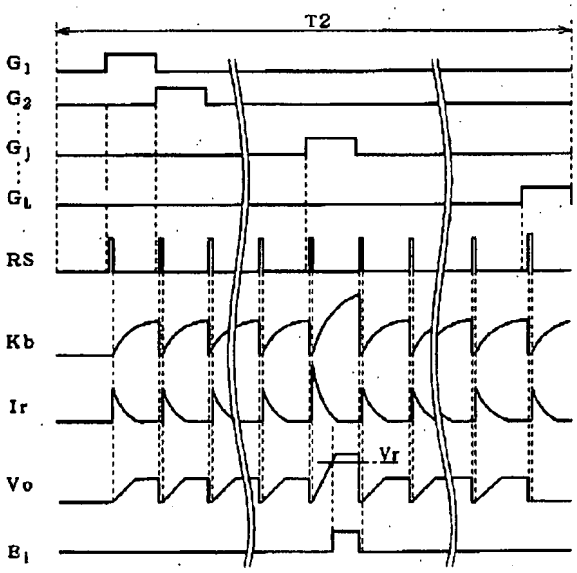
Drawing selection drawing 3



A1 : 積分器
COMP : コンパレータ

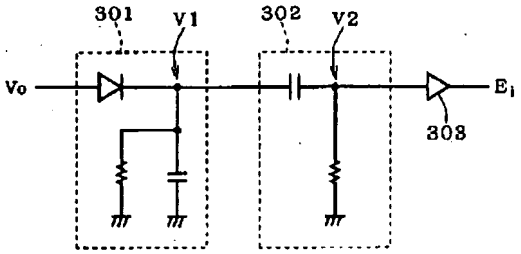
[Translation done.]

Drawing selection drawing 4



[Translation done.]

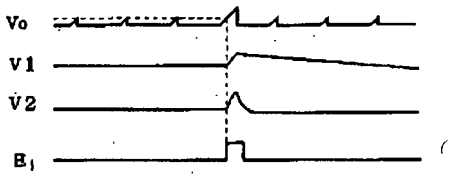
Drawing selection drawing 5



301 : ピークホールド回路
302 : ハイパスフィルタ

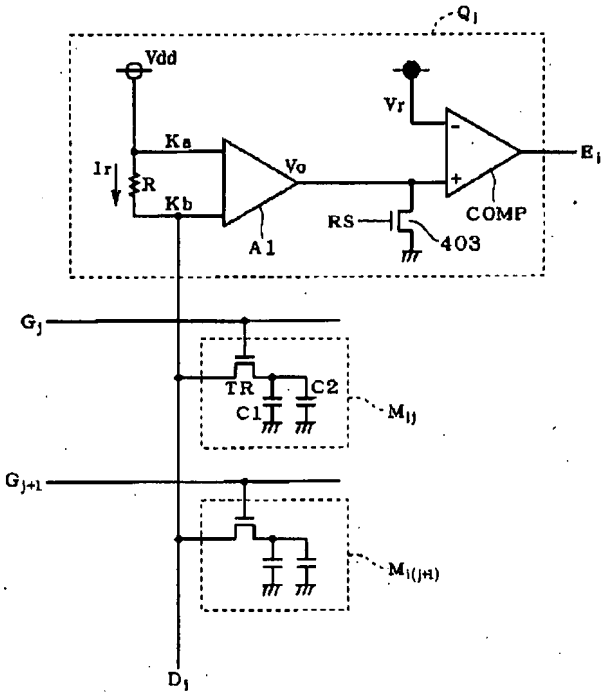
[Translation done.]

Drawing selection drawing 6



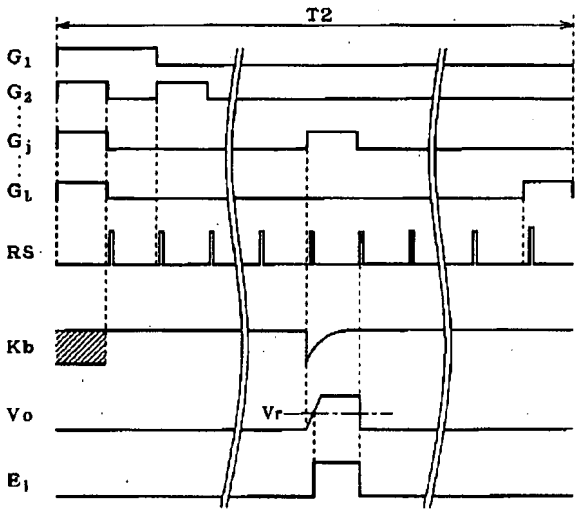
[Translation done.]

Drawing selection drawing 7



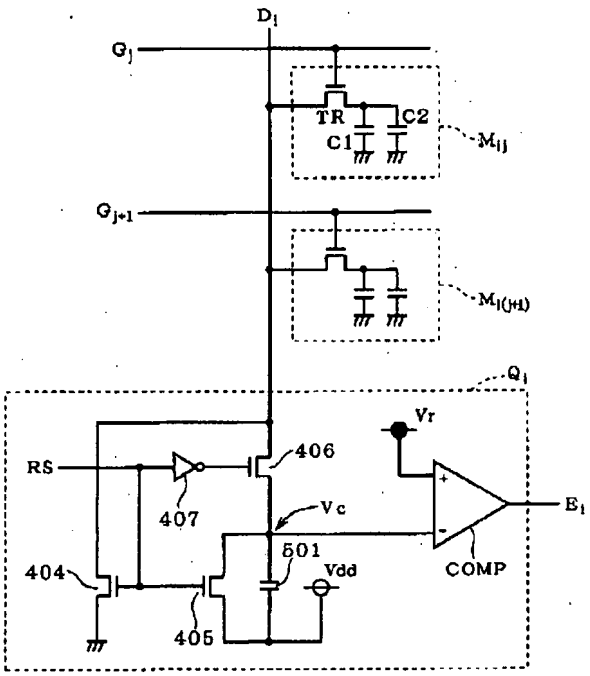
[Translation done.]

Drawing selection drawing 8



[Translation done.]

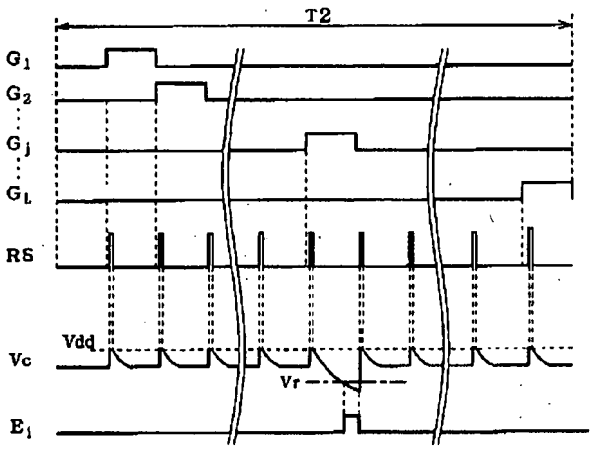
Drawing selection drawing 9



501 : 参照キャパシタ

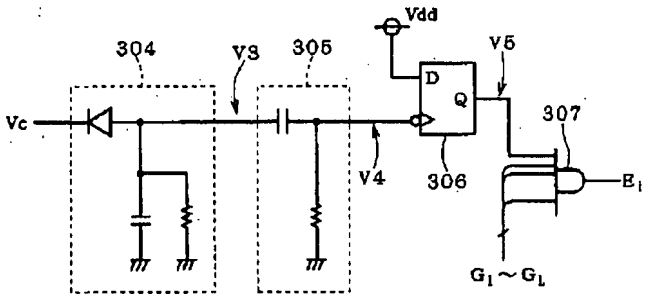
[Translation done.]

Drawing selection drawing 10



[Translation done.]

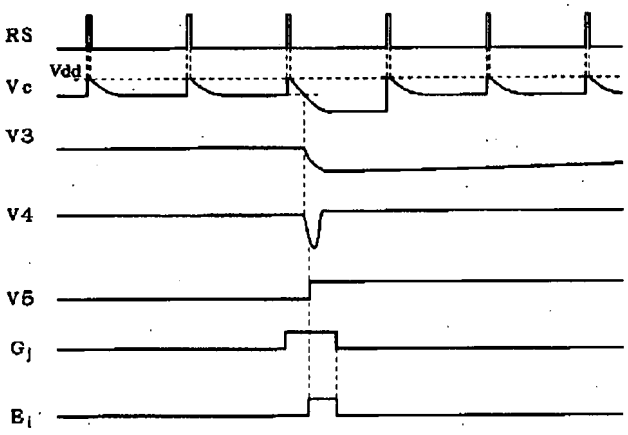
Drawing selection drawing 11



304 ：パレーホールド回路　306 ：Dフリップフロップ
305 ：ハイパスフィルタ

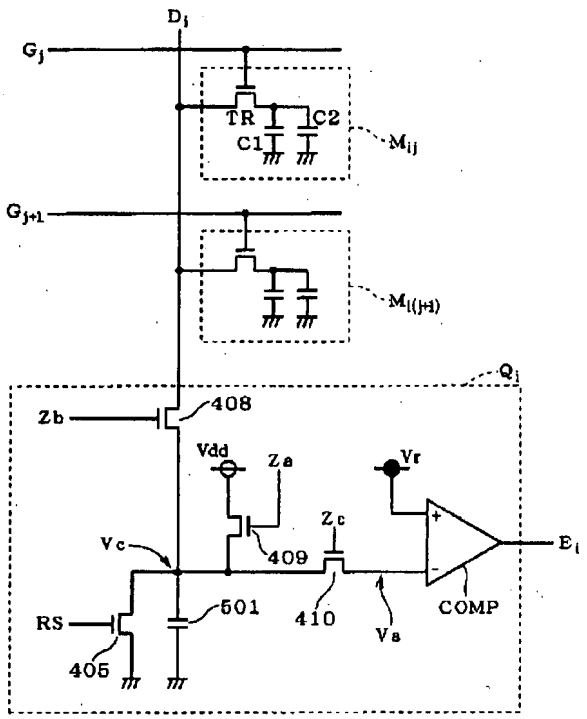
[Translation done.]

Drawing selection drawing 12



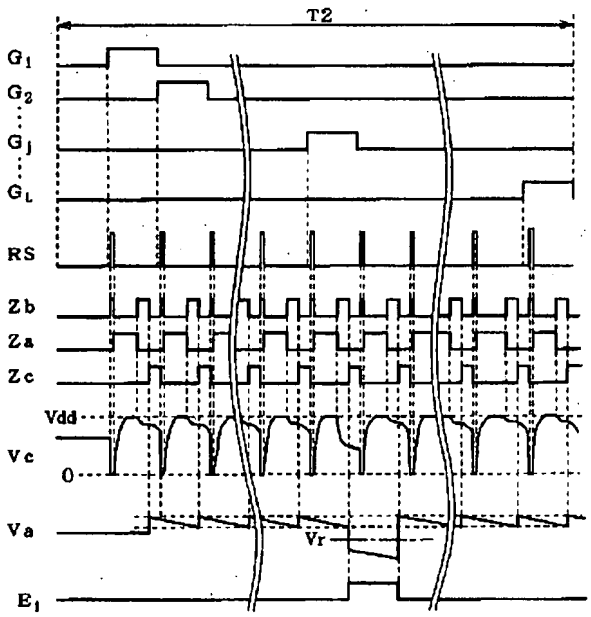
[Translation done.]

Drawing selection drawing 13



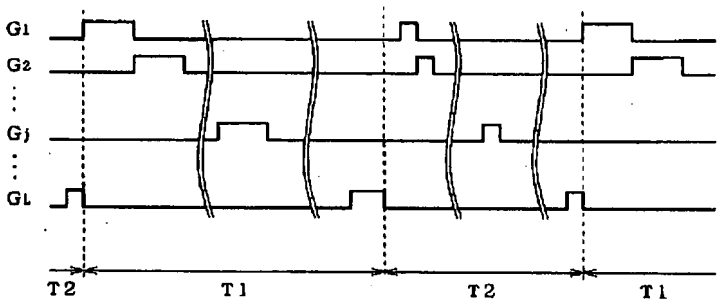
[Translation done.]

Drawing selection drawing 14



[Translation done.]

Drawing selection drawing 15



[Translation done.]